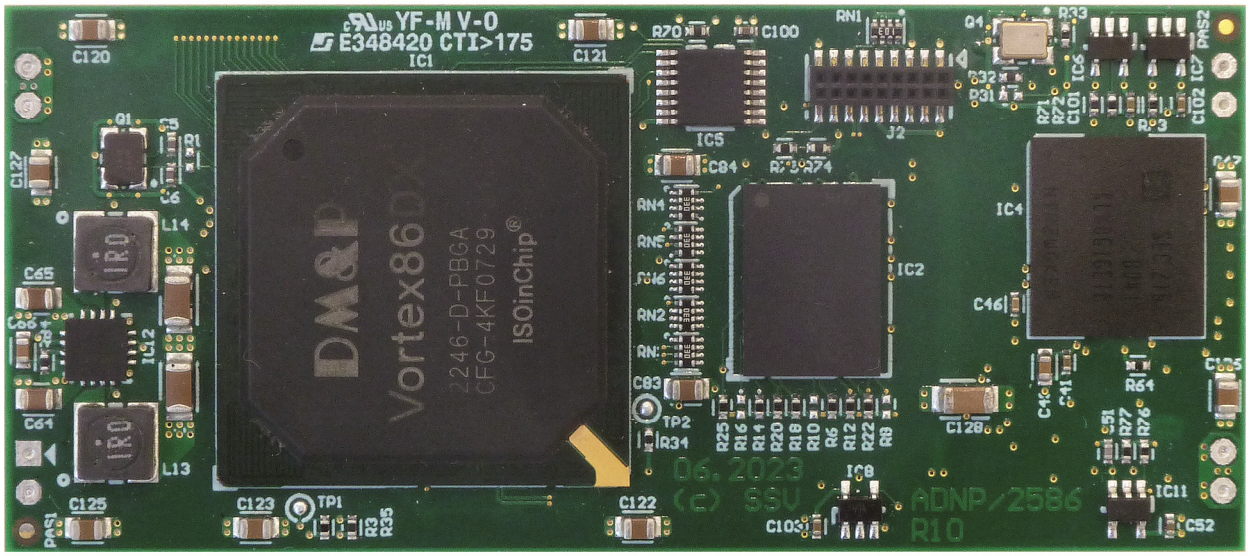
ADVANCED DIL/NETPC

ADNP/2586

Board Revision 1.0



Hardware Reference

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1 INTRODUCTION

This documentation gives an overview about the basic hardware components of the Advanced DIL/NetPC ADNP/2586.

1.1 Checklist

Compare the content of your ADNP/2586 package with the checklist below. If any item is missing or appears to be damaged, please contact SSV.

- ✓ **DIL/NetPC ADNP/2586**

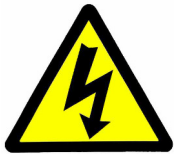
1.2 Document Conventions

Convention	Usage
bold	Important terms
`monospace`	Filenames, Pathnames, program code, command lines

Table 1: Conventions used in this document

2 SAFETY GUIDELINES

Please read the following safety guidelines carefully! In case of property or personal damage by not paying attention to this document and/or by incorrect handling, we do not assume liability. In such cases any warranty claim expires.



ATTENTION!

OBSERVE PRECAUTIONS FOR HANDLING – ELECTROSTATIC SENSITIVE DEVICE!

- **The installation of the device should be done only by qualified personnel.**
- **Discharge yourself electrostatic before you work with the device, e.g. by touching a heater of metal, to avoid damages.**
- **Stay grounded while working with the device to avoid damage through electrostatic discharge.**

3 OVERVIEW

3.1 Block Diagram

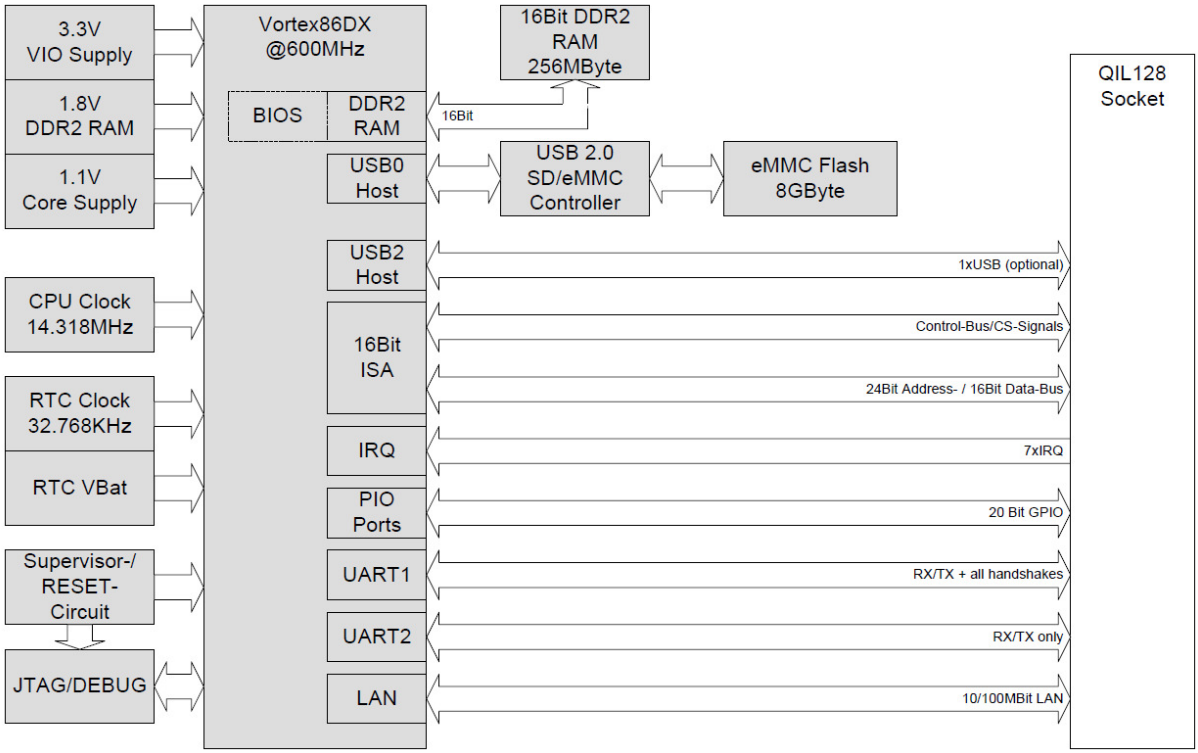


Figure 1: Block diagram of ADNP/2586

3.2 Features and Technical Data

Processor	
Manufacturer / Type	DM&P Vortex86DX 32-bit x86 SoC
Clock speed	600 MHz
BIOS	PC-compatible AMI Basic I/O System
Memory	
RAM	256 MB DDR2 SDRAM (16-bit memory interface)
Storage media	8 GB eMMC mass for operating system and data files
Interfaces	
Ethernet	1x 10/100 Mbps
Serial I/Os	2x 16C550/16C552-compatible UART-based serial ports (one with all handshakes)
GPIOs	20-bit General Purpose Input Output
ISA	16-bit ISA expansion bus with 24 address lines
Interrupts	7x Interrupt inputs
Chip Selects	4x Chip select outputs
Debug	1x 18-pin debug connector
Special Functions	
RTC	1x Real Time Clock
Watchdog	1x Timer watchdog (hardware-based, software-configurable) 1x Power supervisor (hardware-based)
ISP	In-System Programming features
Software	
Operating system	Linux
Electrical Characteristics	
Supply voltage	3.3 VDC ±5%
Supply current	1000 mA typ. @600 MHz
Mechanical Characteristics	
Socket	128-pin JEDEC QIL-128 connector, 2.54 mm centers
Mass	< 50 g
Dimensions	82 mm x 36 mm x 12 mm
Operating temperature	0 .. 60 °C (still air) without heat sink
Standards and Certifications	
EMC	CE
Environmental standards	RoHS, WEEE

Table 2: Technical Data of ADNP/2586

3.3 Board Layout

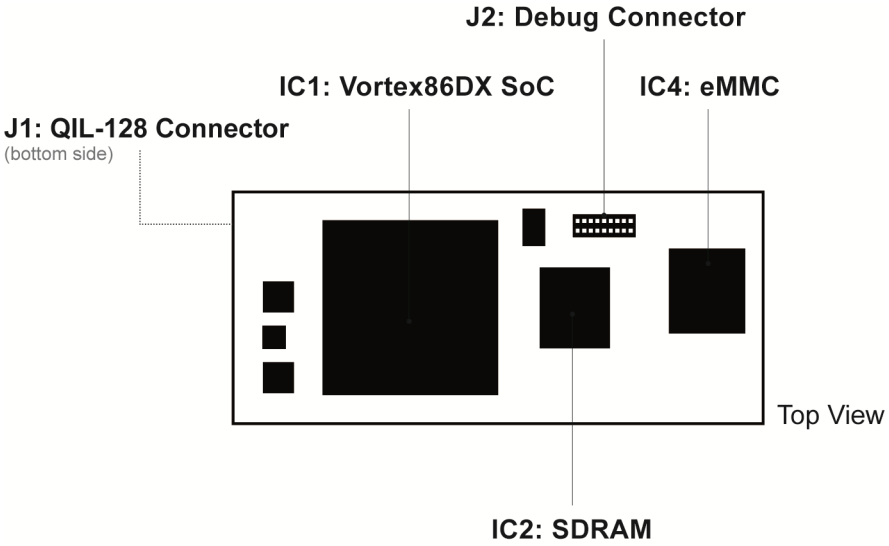


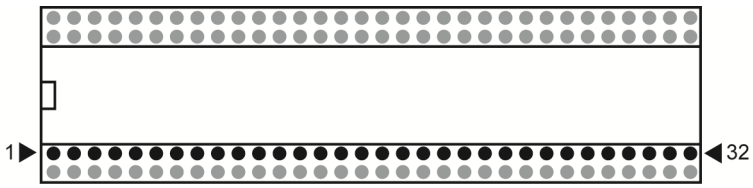
Figure 2: Board layout of ADNP/2586

4 PINOUTS

4.1 QIL-128 Connector – J1

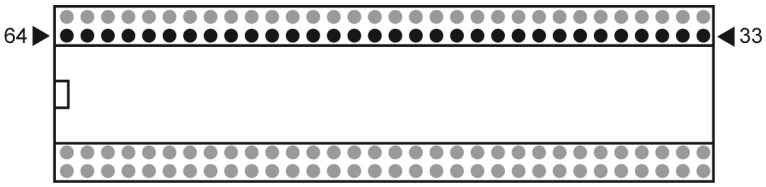
Pin	Name	Group	Function
1	PA0	PIO	Parallel I/O, Port A, Bit 0 *
2	PA1	PIO	Parallel I/O, Port A, Bit 1 *
3	PA2	PIO	Parallel I/O, Port A, Bit 2 *
4	PA3	PIO	Parallel I/O, Port A, Bit 3 *
5	PA4	PIO	Parallel I/O, Port A, Bit 4 *
6	PA5	PIO	Parallel I/O, Port A, Bit 5 *
7	PA6	PIO	Parallel I/O, Port A, Bit 6 *
8	PA7	PIO	Parallel I/O, Port A, Bit 7 *
9	PB0	PIO	Parallel I/O, Port B, Bit 0 *
10	PB1	PIO	Parallel I/O, Port B, Bit 1 *
11	PB2	PIO	Parallel I/O, Port B, Bit 2 *
12	PB3	PIO	Parallel I/O, Port B, Bit 3 *
13	PB4	PIO	Parallel I/O, Port B, Bit 4 *
14	PB5	PIO	Parallel I/O, Port B, Bit 5 *
15	PB6	PIO	Parallel I/O, Port B, Bit 6 *
16	PB7	PIO	Parallel I/O, Port B, Bit 7 *
17	PC0	PIO	Parallel I/O, Port C, Bit 0 *
18	PC1	PIO	Parallel I/O, Port C, Bit 1 *
19	PC2	PIO	Parallel I/O, Port C, Bit 2 *
20	PC3	PIO	Parallel I/O, Port C, Bit 3 *
21	RXD1	SIO	COM1 Serial Port, RXD Pin
22	TXD1	SIO	COM1 Serial Port, TXD Pin
23	CTS1	SIO	COM1 Serial Port, CTS Pin
24	RTS1	SIO	COM1 Serial Port, RTS Pin
25	DCD1	SIO	COM1 Serial Port, DCD Pin
26	DSR1	SIO	COM1 Serial Port, DSR Pin
27	DTR1	SIO	COM1 Serial Port, DTR Pin
28	RI1	SIO	COM1 Serial Port, RI Pin
29	RESIN	RESET	RESET Input
30	TX_P	LAN	10/100 Mbps Ethernet, TX+ Pin
31	TX_N	LAN	10/100 Mbps Ethernet, TX- Pin
32	GND	---	Ground

Table 3: Pinout QIL-128 connector – part 1



Pin	Name	Group	Function
33	RX_P	LAN	10/100 Mbps Ethernet Interface, RX+ Pin
34	RX_N	LAN	10/100 Mbps Ethernet Interface, RX- Pin
35	RESOUT	RESET	RESET Output
36	VBAT	PSP*	Real Time Clock Battery Input
37	CLKOUT	PSP*	Clock Output (option: ISA clock)
38	TXD2	PSP*	COM2 Serial Port, TXD Pin
39	RXD2	PSP*	COM2 Serial Port, RXD Pin
40	INT5	PSP*	Programmable Interrupt Input 5
41	INT4	PSP*	Programmable Interrupt Input 4
42	INT3	PSP*	Programmable Interrupt Input 3
43	INT2	PSP*	Programmable Interrupt Input 2
44	INT1	PSP*	Programmable Interrupt Input 1
45	CS4	PSP*	Programmable Chip Select Output 4
46	CS3	PSP*	Programmable Chip Select Output 3
47	CS2	PSP*	Programmable Chip Select Output 2
48	CS1	PSP*	Programmable Chip Select Output 1
49	IOCHRDY	PSP*	I/O Channel Ready
50	IOR	PSP*	I/O Read Signal, I/O Expansion Bus
51	IOW	PSP*	I/O Write Signal, I/O Expansion Bus
52	SA3	PSP*	System Expansion Bus, Address Bit 3
53	SA2	PSP*	System Expansion Bus, Address Bit 2
54	SA1	PSP*	System Expansion Bus, Address Bit 1
55	SA0	PSP*	System Expansion Bus, Address Bit 0
56	SD7	PSP*	System Expansion Bus, Data Bit 7
57	SD6	PSP*	System Expansion Bus, Data Bit 6
58	SD5	PSP*	System Expansion Bus, Data Bit 5
59	SD4	PSP*	System Expansion Bus, Data Bit 4
60	SD3	PSP*	System Expansion Bus, Data Bit 3
61	SD2	PSP*	System Expansion Bus, Data Bit 2
62	SD1	PSP*	System Expansion Bus, Data Bit 1
63	SD0	PSP*	System Expansion Bus, Data Bit 0
64	VCC	---	3.3 Volt Power Input

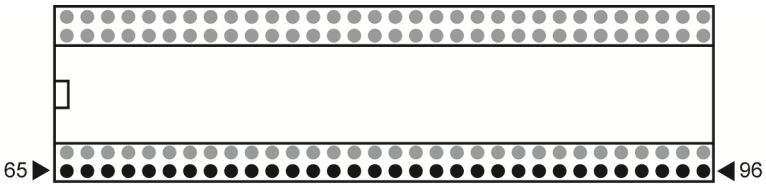
Table 4: Pinout QIL-128 connector – part 2



Please note:
Some pins are called "Product Specific Pins (PSP)". Other members of the DIL/NetPC family will differ with these pins from the ADNP/2586. All other pins will have the same primary functions.

Pin	Name	Group	Function
65	SBHE	PSP*	System Byte High Enable, System Expansion Bus
66	IOCS16	PSP*	I/O Chip Select 16, System Expansion Bus
67	MEMCS16	PSP*	Memory Chip Select 16, System Expansion Bus
68	MEMW	PSP*	Memory Write Signal, System Expansion Bus
69	MEMR	PSP*	Memory Read Signal, System Expansion Bus
70	BALE	PSP*	Bus Latch Enable, System Expansion Bus
71	AEN	PSP*	Address Enable Signal, System Expansion Bus
72	Reserved	PSP*	Reserved – Do not use
73	RCME	PSP*	Remote Console Mode Enable
74	Reserved	PSP*	Reserved – Do not use
75	Reserved	PSP*	Reserved – Do not use
76	Reserved	PSP*	Reserved – Do not use
77	Reserved	PSP*	Reserved – Do not use
78	Reserved	PSP*	Reserved – Do not use
79	Reserved	PSP*	Reserved – Do not use
80	Reserved	PSP*	Reserved – Do not use
81	Reserved	PSP*	Reserved – Do not use
82	Reserved	PSP*	Reserved – Do not use
83	Reserved	PSP*	Reserved – Do not use
84	Reserved	PSP*	Reserved – Do not use
85	INT6	PSP*	Programmable Interrupt Input 6
86	INT7	PSP*	Programmable Interrupt Input 7
87	IDERES	PSP*	IDE Interface Reset Output
88	IDECS0	PSP*	IDE Interface Chip Select 0
89	IDECS1	PSP*	IDE Interface Chip Select 1
90	Reserved	PSP*	Reserved – Do not use
91	Reserved	PSP*	Reserved – Do not use
92	Reserved	PSP*	Reserved – Do not use
93	Reserved	PSP*	Reserved – Do not use
94	Reserved	PSP*	Reserved – Do not use
95	Reserved	PSP*	Reserved – Do not use
96	GND	---	Ground

Table 5: Pinout QIL-128 connector – part 3



Please note:
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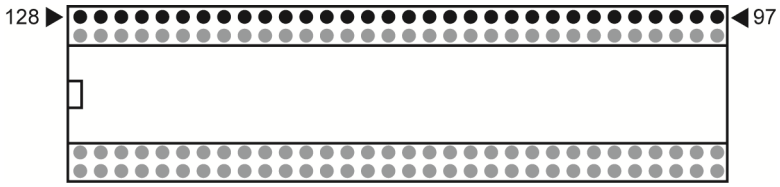
Pin	Name	Group	Function
97	LANLED	PSP*	LAN Interface Activity LED
98	Reserved	PSP*	Reserved – Do not use
99	RSTDRV	PSP*	Reset Output, System Expansion Bus
100	SA23	PSP*	System Expansion Bus, Address Bit 23
101	SA22	PSP*	System Expansion Bus, Address Bit 22
102	SA21	PSP*	System Expansion Bus, Address Bit 21
103	SA20	PSP*	System Expansion Bus, Address Bit 20
104	SA19	PSP*	System Expansion Bus, Address Bit 19
105	SA18	PSP*	System Expansion Bus, Address Bit 18
106	SA17	PSP*	System Expansion Bus, Address Bit 17
107	SA16	PSP*	System Expansion Bus, Address Bit 16
108	SA15	PSP*	System Expansion Bus, Address Bit 15
109	SA14	PSP*	System Expansion Bus, Address Bit 14
110	SA13	PSP*	System Expansion Bus, Address Bit 13
111	SA12	PSP*	System Expansion Bus, Address Bit 12
112	SA11	PSP*	System Expansion Bus, Address Bit 11
113	SA10	PSP*	System Expansion Bus, Address Bit 10
114	SA9	PSP*	System Expansion Bus, Address Bit 9
115	SA8	PSP*	System Expansion Bus, Address Bit 8
116	SA7	PSP*	System Expansion Bus, Address Bit 7
117	SA6	PSP*	System Expansion Bus, Address Bit 6
118	SA5	PSP*	System Expansion Bus, Address Bit 5
119	SA4	PSP*	System Expansion Bus, Address Bit 4
120	SD15	PSP*	System Expansion Bus, Data Bit 15
121	SD14	PSP*	System Expansion Bus, Data Bit 14
122	SD13	PSP*	System Expansion Bus, Data Bit 13
123	SD12	PSP*	System Expansion Bus, Data Bit 12
124	SD11	PSP*	System Expansion Bus, Data Bit 11
125	SD10	PSP*	System Expansion Bus, Data Bit 10
126	SD9	PSP*	System Expansion Bus, Data Bit 9
127	SD8	PSP*	System Expansion Bus, Data Bit 8
128	VCC	---	3.3 Volt Power Input

Table 6: Pinout QIL-128 connector – part 4



Please note:
Some pins are called "Product Specific Pins (PSP)". Other members of the DIL/NetPC family will differ with these pins from the ADNP/2586. All other pins will have the same primary functions.

4.2 Debug Connector – J2

Pin	Name	Function
1	VCC	Power (3.3 VDC I/O voltage)
2	GND	Ground
3	---	Reserved
4	---	Reserved
5	FS1	Factory setup pin 1
6	---	Reserved
7	FS2	Factory setup pin 2
8	---	Reserved
9	FS3	Factory setup pin 3
10	GND	Ground
11	---	Reserved
12	USBF_D_P	USB device data + (eMMC controller)
13	FS4	Factory setup pin 4
14	USBF_D_N	USB device data - (eMMC controller)
15	PWRGD#	Power Good (internal CPU reset)
16	---	Reserved
17	GND	Ground
18	USBF_DIS	Default low (pull high for eMMC access)

Table 7: Pinout debug connector

5 ADDITIONAL INFORMATION

5.1 Signal Description

Signal	Description
PIO_xx	20x GPIO signals
SIO1_xx	8x UART I/O signals
LAN_xx	4x LAN interface I/O signals
RESET_IN	1x System reset signal input
RESET_OUT	1x System reset signal output

Table 8: Signal description of ADNP/2586

Please note:
Refer to **table 9** for more details about the DC electrical characteristics.

5.2 DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIL	Low-Level Input Voltage	---	0	0.8	V
VIH	High-Level Input Voltage	2.5	3.3	---	V
VOL	Low-Level Output Voltage	---	---	0.4	V
VOH	High-Level Output Voltage	2.4	---	VCC_IO	V
IIN	Input leakage current for all input pins (except those with pull up/down resistors)	---	---	±10	µA
IINP	Input leakage current for all input pins with pull up/down resistors	---	---	±44	µA
CPIN	Pin capacitance	---	---	3.1	pF
VBAT	Battery power for RTC	2.0	3	3.3	V
IBAT	Battery standby current for RTC	---	---	1.5	µA

Table 9: DC electrical characteristics of ADNP/2586

5.3 System Memory Mapping

Physical Address Range	Description	Access Format	Type
0x0000.0000 - 0x000F.FFFF	1 MByte DOS/BIOS Area	16-bit MEM R/W	MEM
0x0010.0000 - 0x0FFF.FFFF	255 MByte Main Memory	16-bit MEM R/W	MEM

Table 10: System memory mapping of ADNP/2586

5.4 Interrupt (IRQ) Mapping

ADNP Pin	Vortex86DX
INT1	IRQ5
INT2	IRQ12
INT3	IRQ10
INT4	IRQ6
INT5	IRQ7
INT6	IRQ14
INT7	IRQ11

Table 11: IRQ mapping of ADNP/2586

5.5 Chip Select Mapping

ADNP Pin	Vortex86DX	BIOS Mapping
CS1	0x100 - 0x10F	8-bit IO R/W
CS2	0x110 - 0x11F	8-bit IO R/W
CS3	0x120 - 0x12F	8-bit IO R/W
CS4	0xC8000 - 0xCBFFF	8-bit MEM R/W
IDECS0	0x160 - 0x16F	8-bit IO R/W
IDECS1	0x170 - 0x17F	8-bit IO R/W

Table 12: Chip select mapping of ADNP/2586

5.6 Mechanical Dimensions

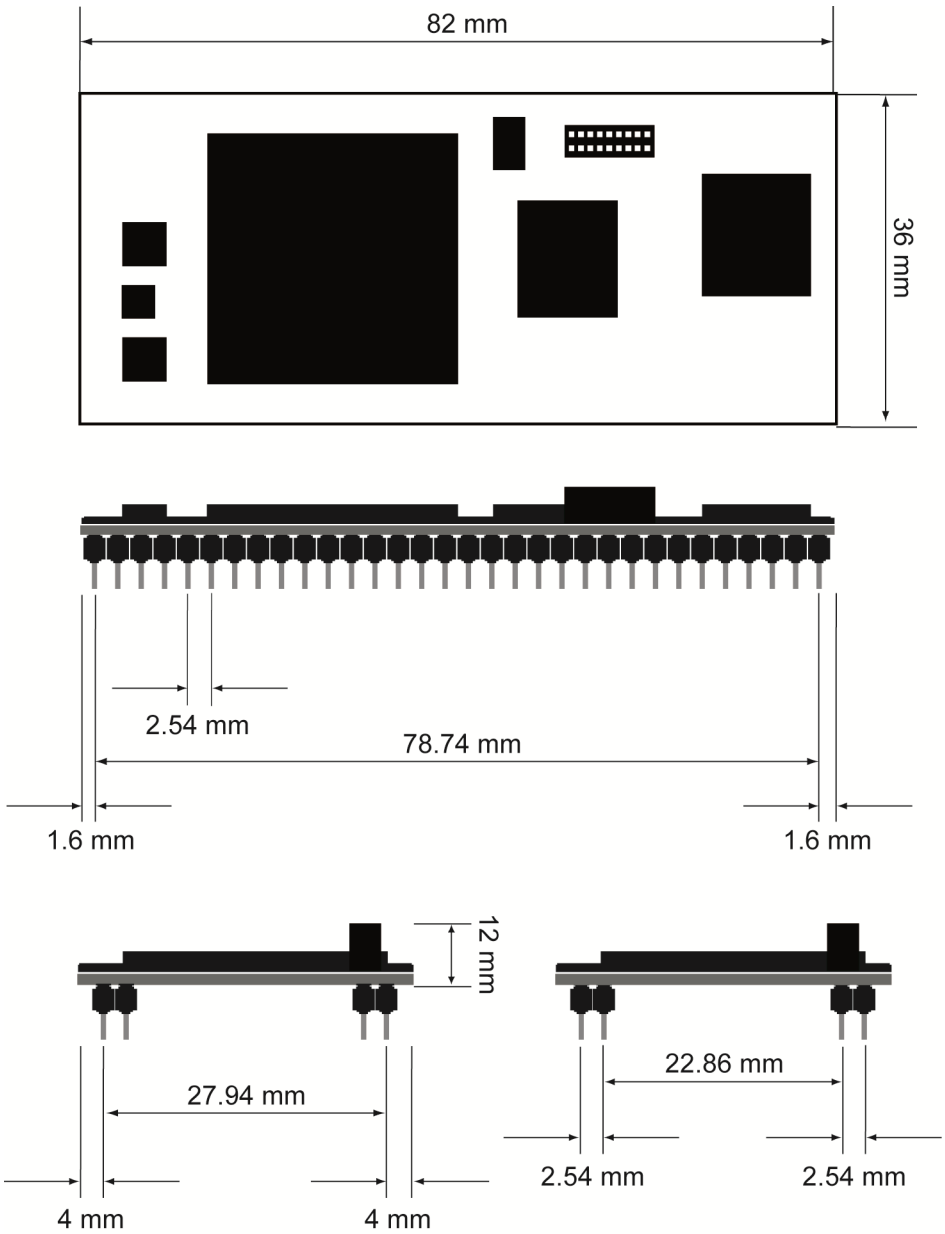


Figure 3: Mechanical dimensions of ADNP/2586

6 HELPFUL LITERATURE

- DM&P Vortex86DX datasheet

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DOCUMENT HISTORY

Revision	Date	Remarks	Name	Review
1.0	2023-08-04	First version	WBU	SSC

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