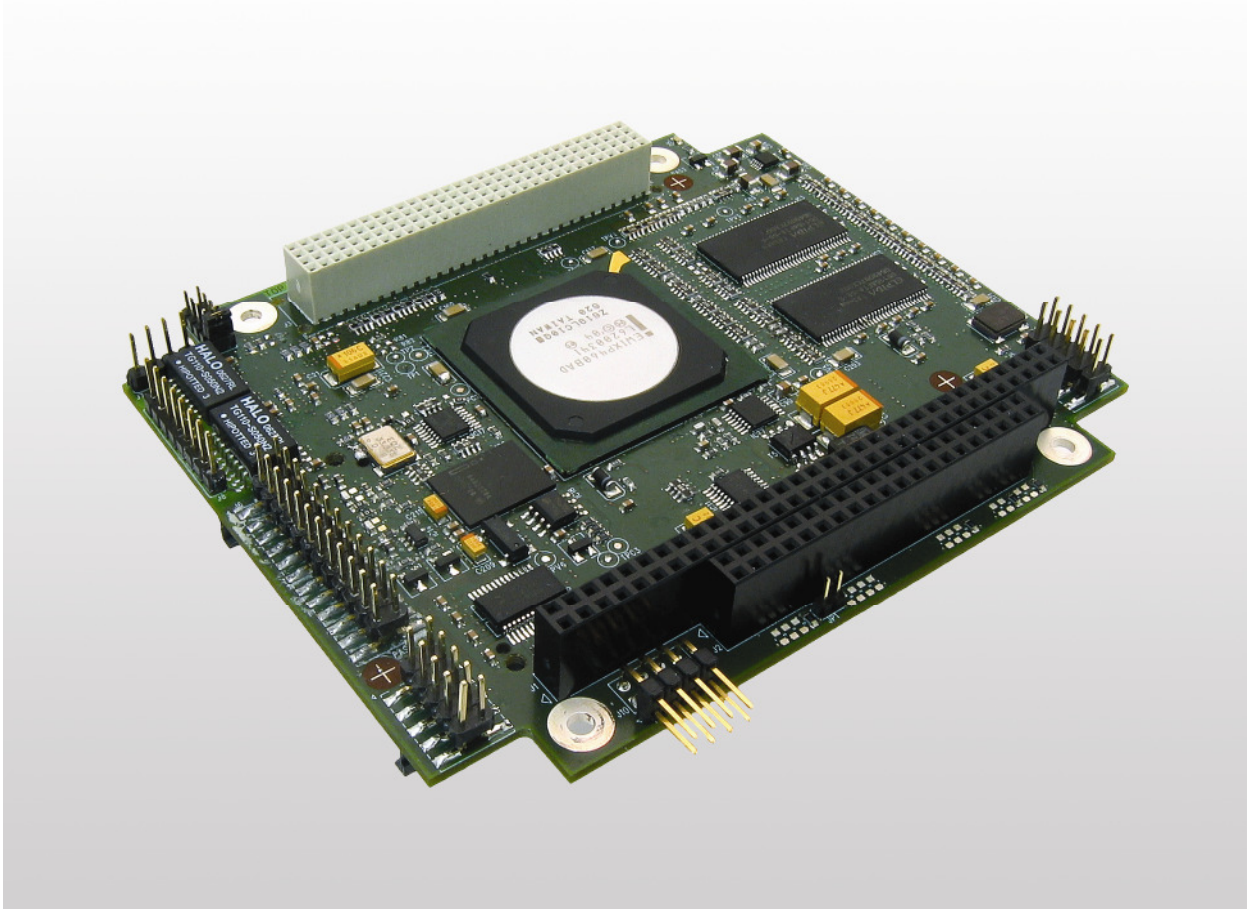
CP/465 PC/104-Plus Board
Board Revision 1.0

Hardware Reference



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Manual Revision: 1.0
Date: 2008-02-19

CONTENT

1 INTRODUCTION

This document describes the hardware components of the CP/465 PC/104-Plus Board. For further information about the individual components of this product you may follow the links from our website at `http://www.ssv-comm.de`. Our website contains a lot of technical information, which will be updated in regular periods.

1.1 Safety Guidelines

Please read the following safety guidelines carefully! In case of property or personal damage by not paying attention to this document and/or by incorrect handling, we do not assume liability. In such cases any warranty claim expires.

ATTENTION: Observe precautions for handling – electrostatic sensitive device!

- Discharge yourself before you work with the device, e.g. by touching a heater of metal, to avoid damages.
- Stay grounded while working with the device to avoid damage through electrostatic discharge.

1.2 Conventions

Convention	Usage
bold	Important terms
italic	Filenames, user inputs and command lines
`monospace`	Pathnames, internet addresses and program code

Table 1: Conventions used in this Document

1.3 Block Diagram

The CP/465 main component is the Intel IXP465 network processor. This microcontroller unit (MCU) contains an Intel Xscale processing core. From the software point of view the Xscale architecture is compatible with ARM. The IXP465 comes as 544-pin PBGA device. The MCU contains a PCI interface, two high-speed UARTs, three Ethernet MAC units and many more features.

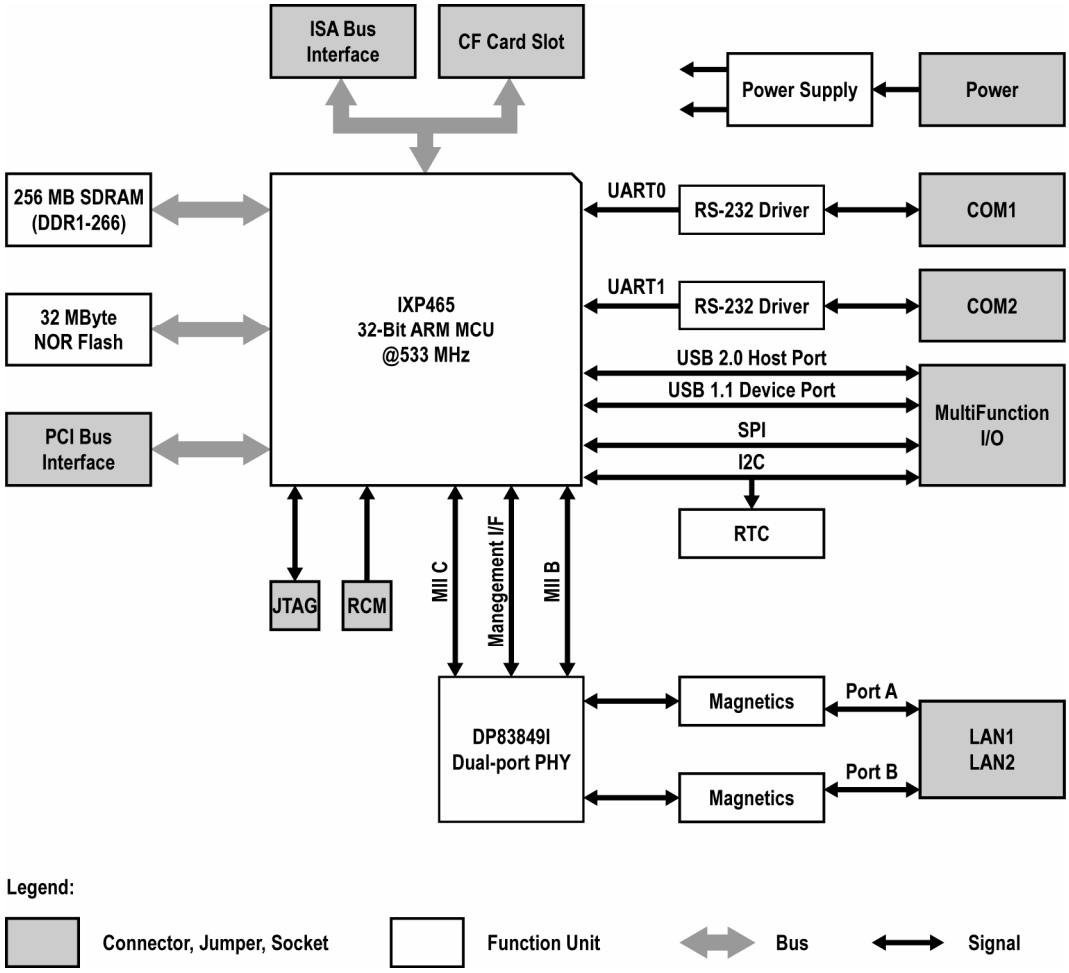


Figure 1: Block diagram of CP/465 PC/104-Plus Board

The two IXP465 MACs – named as MII B and MII C – are connected to an on-board DP83849I dual-port PHY from National Semiconductor. The following table shows the port name mapping for the CP/465:

CP/465 LAN Interface	DP83849I PHY Port	IXP465 MAC Name
LAN1	Port A	MII B
LAN2	Port B	MII C

Table 2: LAN port name mapping of CP/465 PC/104-Plus Board

The DP83849I offers many special features, e.g. port swapping, linked cable status, link quality monitor, cable diagnostic. These features can be used with the help of the management interface.

1.4 Board Features and Technical Data

- Intel 32-bit IXP465 ARM MCU @ 533 MHz
- 256 MByte 32-bit SDRAM memory (DDR1-266)
- 32 MByte NOR FLASH memory for O/S boot image
- 1x CompactFlash (CF) card slot
- 2x 10/100 Mbps Ethernet LAN interface with Auto-MDIX support
- DP83849I Dual-port PHY with port switching and monitoring support
- Allows Ethernet ring topology (Industrial Ethernet Ring)
- IEEE 1588 PTP for Precision Clock Synchronization Protocol
- Ethernet cable diagnostic support
- 1x I2C (Inter Integrated Circuit) bus interface
- 1x SPI (Serial Peripheral Interface) with one chip select output
- 1x USB host interface
- 1x USB device interface
- 2x UART-based high-speed serial ports (up to 921 Kbps)
- 16-bit PC/104 ISA expansion bus connector
- 32-bit PC/104 PCI expansion bus connector with 33 MHz PCI signals
- Preinstalled boot loader and Embedded Linux O/S
- Programmable Watchdog Timer
- JTAG IEEE 1149.1 test interface
- In-System Programming features
- Low power design, supply voltage 5 VDC (±5 %)
- 0 °C to +70 °C operating temperature
- RoHS conform

1.5 MCU and PHY Features

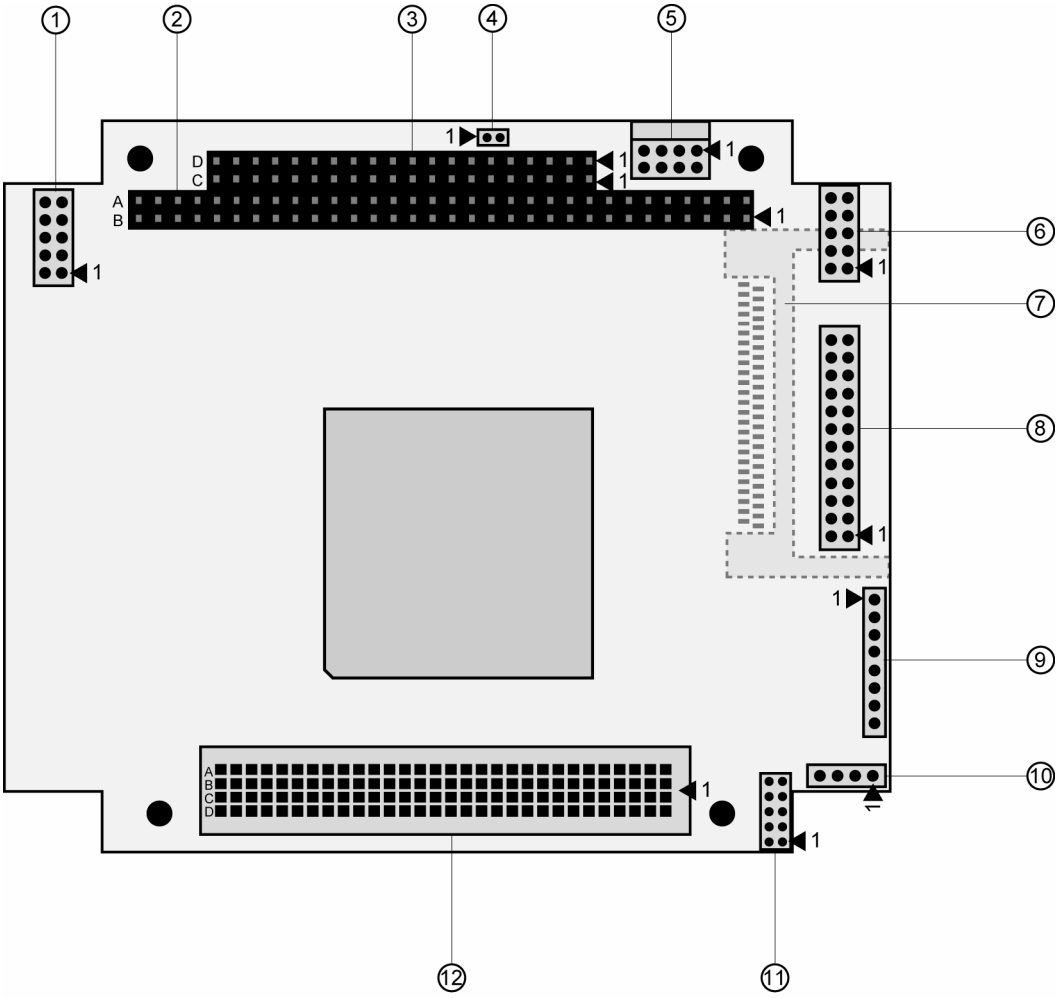
The IXP465 microcontroller unit from Intel is a feature-rich 32-bit MCU for high-speed networking router and gateway applications. The most important features are:

- ARM processor core @533 MHz (Intel XScale-based)
- PCI v. 2.2 33/66 MHz interface
- DDRI SDRAM interface
- USB 1.1 device controller
- USB 2.0 host controller
- SPI/I2C interfaces
- Two high-speed UART interfaces
- Up to three MII interfaces
- Cryptography unit (random number generator and exponentiation unit)
- Encryption/Authentication unit (AES/AES-CCM/3DES/DES/SHA-1/SHA-256/SHA-384/SHA-512/MD-5)
- IEEE 1588 PTP hardware assist

The CP/465 DP83849I dual-port PHY from National Semiconductor offers some special features for industrial networking applications. The DP83849I supports Ethernet ring topologies (Industrial Ethernet Ring) and redundant connections for mission-critical applications. Other special features are:

- Management interface (single register access for complete PHY status)
- Auto-MDIX for 10/100 Mbps
- Energy detection mode
- Flexible MII port assignment
- Dynamic link quality monitoring
- Cable diagnostic and cable length detection
- 10/100 Mbps packet BIST (Built-in Self Test)

2 BOARD LAYOUT



① J5 - COM2 connector
② J1 - PC/104 64-pin ISA interface
③ J2 - PC/104 40-pin ISA interface
④ JP1 - RCM jumper
⑤ J10 - Power connector
⑥ J4 - COM1 connector
⑦ J9 - CompactFlash slot (bottom side)
⑧ J6 - MultiFunction I/O connector
⑨ J8 - LAN1/2 connector
⑩ J7 - LAN LED connector
⑪ J11 - Service/JTAG connector
⑫ J3 - PC/104 120-pin PCI interface

Table 3: Board layout CP/465 PC/104-Plus Board

3 PINOUTS

3.1 ISA Bus Interface – J1/P1 (Row A)

Pin	Name	Function
1	IOCHCK#	I/O Channel Check
2	SD7	Serial Data Bit 7
3	SD6	Serial Data Bit 6
4	SD5	Serial Data Bit 5
5	SD4	Serial Data Bit 4
6	SD3	Serial Data Bit 3
7	SD2	Serial Data Bit 2
8	SD1	Serial Data Bit 1
9	SD0	Serial Data Bit 0
10	IOCHRDY	I/O Channel Ready
11	AEN	Address Enable
12	SA19	Serial Address Bit 19
13	SA18	Serial Address Bit 18
14	SA17	Serial Address Bit 17
15	SA16	Serial Address Bit 16
16	SA15	Serial Address Bit 15
17	SA14	Serial Address Bit 14
18	SA13	Serial Address Bit 13
19	SA12	Serial Address Bit 12
20	SA11	Serial Address Bit 11
21	SA10	Serial Address Bit 10
22	SA9	Serial Address Bit 9
23	SA8	Serial Address Bit 8
24	SA7	Serial Address Bit 7
25	SA6	Serial Address Bit 6
26	SA5	Serial Address Bit 5
27	SA4	Serial Address Bit 4
28	SA3	Serial Address Bit 3
29	SA2	Serial Address Bit 2
30	SA1	Serial Address Bit 1
31	SA0	Serial Address Bit 0
32	GND	Ground

Table 4: Pinout ISA bus interface – row A

3.2 ISA Bus Interface – J1/P1 (Row B)

Pin	Name	Function
1	GND	Ground
2	RESET	Reset Input
3	+5V	+5 VDC Power Output
4	IRQ9	Interrupt Request 9
5	-5V	-5 VDC Power Output
6	DRQ2	DMA Request 2
7	-12V	-12 VDC Power Output
8	SRDY#	Synchronous Ready (or NOWS# No-Wait-State)
9	+12V	+12 VDC Power Output
10	KEY	Ground
11	SMEMW#	System Memory Write
12	SMEMR#	System Memory read
13	IOW#	I/O Write
14	IOR#	I/O Read
15	DACK3#	DMA Acknowledge 3
16	DRQ3	DMA Request 3
17	DACK1#	DMA Acknowledge 1
18	DRQ1	DMA Request 1
19	REFRESH#	Memory Refresh
20	BCLK	System Bus Clock
21	IRQ7	Interrupt Request 7
22	IRQ6	Interrupt Request 6
23	IRQ5	Interrupt Request 5
24	IRQ4	Interrupt Request 4
25	IRQ3	Interrupt Request 3
26	DACK2#	DMA Acknowledge 2
27	TC	Terminal Count
28	BALE	Bus Address Latch Enable
29	+5V	+5 VDC Power Output
30	OSC	Oscillator
31	GND	Ground
32	GND	Ground

Table 5: Pinout ISA bus interface – row B

3.3 ISA Bus Interface – J2/P2 (Row C)

Pin	Name	Function
0	GND	Ground
1	SBHE#	System Byte High Enable
2	LA23	Latched Address 23
3	LA22	Latched Address 22
4	LA21	Latched Address 21
5	LA20	Latched Address 20
6	LA19	Latched Address 19
7	LA18	Latched Address 18
8	LA17	Latched Address 17
9	MEMR#	Memory Read
10	MEMW#	Memory Write
11	SD8	Serial Data Bit 8
12	SD9	Serial Data Bit 9
13	SD10	Serial Data Bit 10
14	SD11	Serial Data Bit 11
15	SD12	Serial Data Bit 12
16	SD13	Serial Data Bit 13
17	SD14	Serial Data Bit 14
18	SD15	Serial Data Bit 15
19	KEY	Ground

Table 6: Pinout ISA bus interface – row C

3.4 ISA Bus Interface – J2/P2 (Row D)

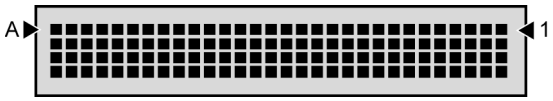
Pin	Name	Function
0	GND	Ground
1	MEMCS16#	Memory Chip Select 16
2	IOCS16#	I/O Chip Select 16
3	IRQ10	Interrupt Request 10
4	IRQ11	Interrupt Request 11
5	IRQ12	Interrupt Request 12
6	IRQ15	Interrupt Request 15
7	IRQ14	Interrupt Request 14
8	DACK0#	DMA Acknowledge 0
9	DRQ0	DMA Request 0
10	DACK5#	DMA Acknowledge 5
11	DRQ5	DMA Request 5
12	DACK6#	DMA Acknowledge 6
13	DRQ6	DMA Request 6
14	DACK7#	DMA Acknowledge 7
15	DRQ7	DMA Request 7
16	+5V	+5 VDC Power Output
17	MASTER#	Master 16
18	GND	Ground
19	GND	Ground

Table 7: Pinout ISA bus interface – row D

3.5 PCI Bus Interface – J3/P3 (Row A)

Pin	Name	Function
1	GND	Ground
2	VI/O	3.3 VDC Power Output for 3.3 VDC PCI Devices
3	AD05	Address and Data Bit 5
4	C/BE0#	Bus Command/Byte Enables 0
5	GND	Ground
6	AD11	Address and Data Bit 11
7	AD14	Address and Data Bit 14
8	+3.3V	+3.3 VDC Power Output
9	SERR#	System Error
10	GND	Ground
11	STOP#	Stop Current Transaction
12	+3.3V	+3.3 VDC Power Output
13	FRAME#	Cycle Frame
14	GND	Ground
15	AD18	Address and Data Bit 18
16	AD21	Address and Data Bit 21
17	+3.3V	+3.3 VDC Power Output
18	IDSEL0	Initialization Device Select 0
19	AD24	Address and Data Bit 24
20	GND	Ground
21	AD29	Address and Data Bit 29
22	+5V	+5 VDC Power Output
23	REQ0#	Bus Master Request 0
24	GND	Ground
25	GNT1#	Bus Master Grant 1
26	+5V	+5 VDC Power Output
27	CLK2	PCI Bus Clock 2
28	GND	Ground
29	+12V	+12 VDC Power Output
30	-12V	-12 VDC Power Output

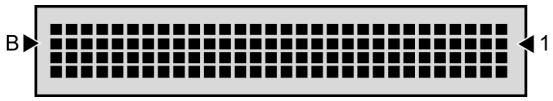
Table 8: Pinout PCI bus interface – row A



3.6 PCI Bus Interface – J3/P3 (Row B)

Pin	Name	Function
1	---	Reserved
2	AD02	Address and Data Bit 2
3	GND	Ground
4	AD07	Address and Data Bit 7
5	AD09	Address and Data Bit 9
6	VI/O	Determine PCI Signal Level (3.3 VDC PCI Devices only)
7	AD13	Address and Data Bit 13
8	C/BE1#	Bus Command/Byte Enables 1
9	GND	Ground
10	PERR#	Parity Error
11	+3.3V	+3.3 VDC Power Output
12	TRDY#	Target Ready
13	GND	Ground
14	AD16	Address and Data Bit 16
15	+3.3V	+3.3 VDC Power Output
16	AD20	Address and Data Bit 20
17	AD23	Address and Data Bit 23
18	GND	Ground
19	C/BE3#	Bus Command/Byte Enables 3
20	AD26	Address and Data Bit 26
21	+5V	+5 VDC Power Output
22	AD30	Address and Data Bit 30
23	GND	Ground
24	REQ2#	Bus Master Request 2
25	VI/O	Determine PCI Signal Level (3.3 VDC PCI Devices only)
26	CLK0	PCI Bus Clock 0
27	+5V	+5 VDC Power Output
28	INTD#	Interrupt D
29	INTA#	Interrupt A
30	REQ3#	Bus Master Request 3

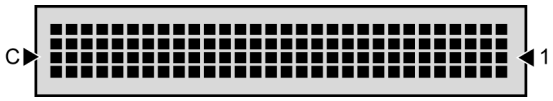
Table 9: Pinout PCI bus interface – row B



3.7 PCI Bus Interface – J3/P3 (Row C)

Pin	Name	Function
1	+5V	+5 VDC Power Output
2	AD01	Address and Data Bit 1
3	AD04	Address and Data Bit 4
4	GND	Ground
5	AD08	Address and Data Bit 8
6	AD10	Address and Data Bit 10
7	GND	Ground
8	AD15	Address and Data Bit 15
9	---	Reserved
10	+3.3V	+3.3 VDC Power Output
11	LOCK#	Lock
12	GND	Ground
13	IRDY#	Initiator Ready
14	+3.3V	+3.3 VDC Power Output
15	AD17	Address and Data Bit 17
16	GND	Ground
17	AD22	Address and Data Bit 22
18	IDSEL1	Initialization Device Select 1
19	VI/O	Determine PCI Signal Level (3.3 VDC PCI Devices only)
20	AD25	Address and Data Bit 25
21	AD28	Address and Data Bit 28
22	GND	Ground
23	REQ1#	Bus Master Request 1
24	+5V	+5 VDC Power Output
25	GNT2#	Bus Master Grant 2
26	GND	Ground
27	CLK3	PCI Bus Clock 3
28	+5V	+5 VDC Power Output
29	INTB#	Interrupt B
30	GNT3#	Bus Master Grant 3

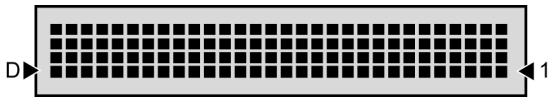
Table 10: Pinout PCI bus interface – row C



3.8 PCI Bus Interface – J3/P3 (Row D)

Pin	Name	Function
1	AD00	Address and Data Bit 0
2	+5V	+5 VDC Power Output
3	AD03	Address and Data Bit 3
4	AD06	Address and Data Bit 6
5	GND	Ground
6	M66EN	66 MHz Enable
7	AD12	Address and Data Bit 12
8	+3.3V	+3.3 VDC Power Output
9	PAR	Parity
10	---	Reserved
11	GND	Ground
12	DEVSEL#	Device Select
13	+3.3V	+3.3 VDC Power Output
14	C/BE2#	Bus Command/Byte Enables 2
15	GND	Ground
16	AD19	Address and Data Bit 19
17	+3.3V	+3.3 VDC Power Output
18	IDSEL2	Initialization Device Select 2
19	IDSEL3	Initialization Device Select 3
20	GND	Ground
21	AD27	Address and Data Bit 27
22	AD31	Address and Data Bit 31
23	VI/O	Determine PCI Signal Level (3.3 VDC PCI Devices only)
24	GNT0#	Bus Master Grant 0
25	GND	Ground
26	CLK1	PCI Bus Clock 1
27	GND	Ground
28	RST#	Reset Input
29	INTC#	Interrupt C
30	GND	Ground

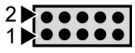
Table 11: Pinout PCI bus interface – row D



3.9 COM1 Connector – J4

Pin	Name	Function
1	DCD1	COM1 Serial Port, DCD Pin (RS232)
2	DSR1	COM1 Serial Port, DSR Pin (RS232)
3	RXD1	COM1 Serial Port, RXD Pin (RS232)
4	RTS1	COM1 Serial Port, RTS Pin (RS232)
5	TXD1	COM1 Serial Port, TXD Pin (RS232)
6	CTS1	COM1 Serial Port, CTS Pin (RS232)
7	DTR1	COM1 Serial Port, DTR Pin (RS232)
8	RI1	COM1 Serial Port, RI Pin (RS232)
9	GND	Ground
10	---	Not Connected

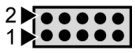
Table 12: Pinout COM1 connector



3.10 COM2 Connector – J5

Pin	Name	Function
1	DCD2	COM2 Serial Port, DCD Pin (RS232)
2	DSR2	COM2 Serial Port, DSR Pin (RS232)
3	RXD2	COM2 Serial Port, RXD Pin (RS232)
4	RTS2	COM2 Serial Port, RTS Pin (RS232)
5	TXD2	COM2 Serial Port, TXD Pin (RS232)
6	CTS2	COM2 Serial Port, CTS Pin (RS232)
7	DTR2	COM2 Serial Port, DTR Pin (RS232)
8	RI2	COM2 Serial Port, RI Pin (RS232)
9	GND	Ground
10	---	Not Connected

Table 13: Pinout COM2 connector



3.11 MultiFunction I/O Connector – J6

Pin	Name	Function
1	---	Not Connected
2	---	Not Connected
3	HD_GND	USB Host Ground
4	DD_GND	USB Device Ground
5	HDP	USB Host Port+
6	DDP	USB Device Port+
7	HDM	USB Host Port-
8	DDM	USB Device Port-
9	HD_VCC	USB Host Power Output
10	DD_VCC	USB Device Power Input
11	VCC3	3.3 VDC Power Output*
12	GND	Ground
13	SPI_MOSI	Master Out Slave In (SPI Data)
14	SPI_MISO	Master In Slave Out (SPI Data)
15	SPI_CLK	SPI Clock
16	SPI_CS0	SPI Chip Select
17	VCC3	3.3 VDC Power Output*
18	GND	Ground
19	I2C_SDA	I2C Data
20	I2C_SCL	I2C Clock
21	GND	Ground
22	GND	Ground
23	RESET#	Reset Input
24	VBAT	Real Time Clock Battery Input

Table 14: Pinout MultiFunction I/O connector

* Power supply for external I2C/SPI devices (max. 200 mA)

3.12 LAN LED Connector – J7

Pin	Name	Function
1	LAN1_LNK#	LAN1 Link/Activity
2	VCC3	3.3 VDC Power Output for external LED
3	VCC3	3.3 VDC Power Output for external LED
4	LAN2_LNK#	LAN2 Link/Activity

Table 15: Pinout LAN LED connector

3.13 LAN1/2 Connector – J8

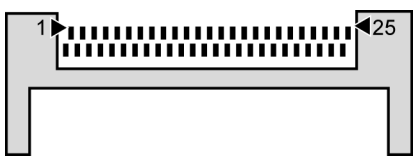
Pin	Name	Function
1	LAN1_RXD-	LAN1, RXD- Pin
2	LAN1_RXD+	LAN1, RXD+ Pin
3	LAN1_TXD-	LAN1, TXD- Pin
4	LAN1_TXD+	LAN1, TXD+ Pin
5	LAN2_RXD-	LAN2, RXD- Pin
6	LAN2_RXD+	LAN2, RXD+ Pin
7	LAN2_TXD-	LAN2, TXD- Pin
8	LAN2_TXD+	LAN2, TXD+ Pin

Table 16: Pinout LAN1/2 connector

3.14 CompactFlash Slot – J9 (1. Part)

Pin	Name	Function
1	GND	Ground
2	D3	Data Bit 3
3	D4	Data Bit 4
4	D5	Data Bit 5
5	D6	Data Bit 6
6	D7	Data Bit 7
7	CS0#	Chip Select 0
8	A10	Connected to Ground
9	ATASEL#	Connected to Ground
10	A9	Connected to Ground
11	A8	Connected to Ground
12	A7	Connected to Ground
13	VCC	3.3 VDC Power Output
14	A6	Connected to Ground
15	A5	Connected to Ground
16	A4	Connected to Ground
17	A3	Connected to Ground
18	A2	Address Bit 2
19	A1	Address Bit 1
20	A0	Address Bit 0
21	D0	Data Bit 0
22	D1	Data Bit 1
23	D2	Data Bit 2
24	IOCS16#	Not Connected
25	CD2#	Not Connected

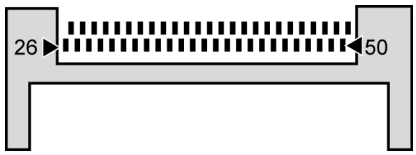
Table 17: Pinout CompactFlash slot – pin 1 to 25



3.15 CompactFlash Slot – J9 (2. Part)

Pin	Name	Function
26	CD1	Not Connected
27	D11	Data Bit 11
28	D12	Data Bit 12
29	D13	Data Bit 13
30	D14	Data Bit 14
31	D15	Data Bit 15
32	CS1#	Chip Select 1
33	VS1#	Not Connected
34	IOR#	Read Strobe
35	IOW#	Write Strobe
36	WE#	Write Enable
37	INTRQ	Interrupt Request
38	VCC	3.3 VDC Power Output
39	CSEL#	Cable Select
40	VS2#	Not Connected
41	RESET#	Reset Pin
42	IORDY	I/O Ready
43	DMARQ	Not Connected
44	DMACK#	DMA Acknowledge
45	DASP#	Device Active or Slave Present
46	PDIAG#	Passed Diagnostics
47	D8	Data Bit 8
48	D9	Data Bit 9
49	D10	Data Bit 10
50	GND	Ground

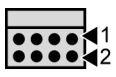
Table 18: Pinout CompactFlash slot – pin 26 to 50



3.16 Power Connector – J10

Pin	Name	Function
1	GND	Ground
2	VCC5	5 VDC Power Input
3	---	Not Connected
4	VCC12	12 VDC Power Input
5	---	Not Connected
6	---	Not Connected
7	GND	Ground
8	VCC5	5 VDC Power Input

Table 19: Pinout power connector



3.17 Service/JTAG Connector – J11

Pin	Name	Function
1	TDI	Test Data In
2	TDO	Test Data Out
3	TMS	Test Mode Select
4	GND	Ground
5	TRST#	Test Reset
6	TCK	Test Clock
7	VCC3	3.3 VDC Power Output
8	---	Not connected
9	WDDIS#	Watchdog Disable
10	GND	Ground

Table 20: Pinout service/JTAG connector

3.18 RCM Jumper – JP1

The **RCM (Remote Console Mode)** offers the possibility to control the CP/465 via a terminal emulation program over the UART-based serial port COM1.

Please note: The default setting of the RCM jumper is set. If you set the RCM jumper you will be able to update the Linux system on the CP/465 over COM1.

To disable RCM remove the jumper cap of the RCM jumper. This frees UART based serial port COM1 for application usage.

RCM jumper	Function
Not set	Disable Remote Console Mode
Set (default)	Enable Remote Console Mode

Table 21: RCM jumper settings

4 MEMORY MAP

Start Address	End Address	Size	Use
0x0000.0000	0x0FFF.FFFF	256 MB	Expansion bus (Boot up)
0x0000.0000	0x0FFF.FFFF	256 MB	DDR1 SDRAM
0x1000.0000	0x3FFF.FFFF	768 MB	Reserved
0x4000.0000	0x47FF.FFFF	128 MB	Reserved
0x4800.0000	0x4FFF.FFFF	128 MB	PCI
0x5000.0000	0x5FFF.FFFF	256 MB	Flash, expansion bus
0x6000.0000	0x63FF.FFFF	64 MB	Queue manager
0xC000.0000	0xCFFF.FFFF	256 MB	Special function register

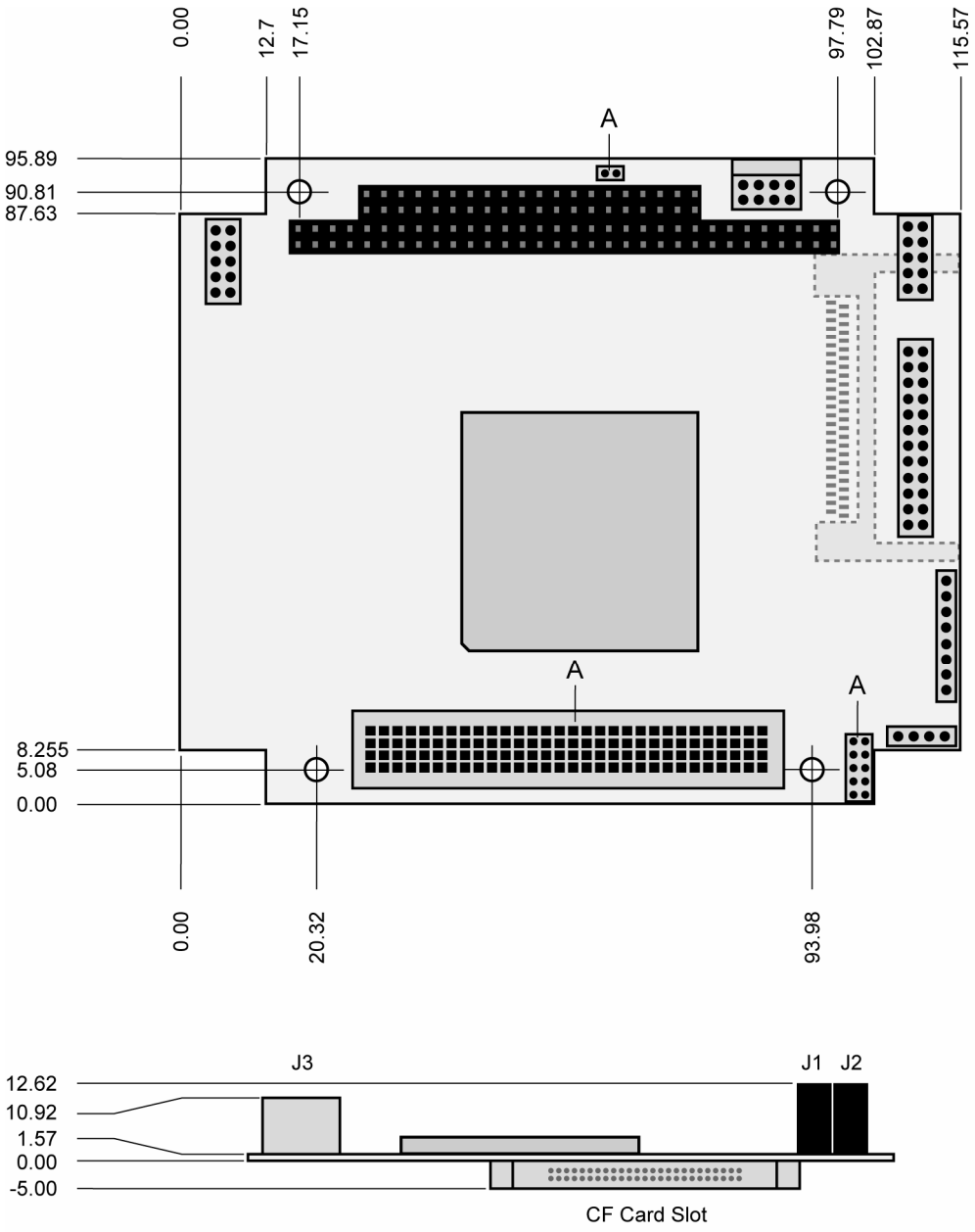
Table 22: CP/465 memory map

Start Address	End Address	Use
0x5000.0000	0x5005.FFFF	RedBoot boot loader (384 Kbyte)
0x5006.0000	0x501B.FFFF	Linux kernel (1.408 Kbyte)
0x501C.0000	0x503B.FFFF	Root file system (2.048 Kbyte)
0x503C.0000	0x50BB.FFFF	Mounted JFFS space (8.192 Kbyte)
0x50BC.0000	0x51FF.FFFF	Free for user demand (20.736 Kbyte)

Table 23: CP/465 Flash usage map

5 MECHANICAL DIMENSIONS

All length dimensions are in millimeters and have a tolerance of 0.5 mm. The drillings are suitable for M3 screws.



A = 2.0 mm raster (all other connectors have a 2.54 mm raster)

Figure 2: Mechanical dimensions of CP/465 PC/104-Plus Board

6 HELPFUL LITERATURE

- IXP465 ARM MCU data sheet (Intel)
- IXP465 ARM MCU developer's manual (Intel)
- IXP465 ARM MCU core developer's manual (Intel)
- DP83849I Dual-port PHY data sheet (National Semiconductor)
- PC/104 specification (`www.pc104.org`)
- PC/104-Plus specification (`www.pc104.org`)

Please note: Intel calls the IXP465 ARM MCU core "XScale®". The XScale MCU architecture is ARM-based. The GNU software tools for the CP/465 Linux are also ARM-based.

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For actual information about the CP/465 PC/104-Plus Board visit us at `www.ssv-comm.de`.

DOCUMENT HISTORY

Revision	Date	Remarks	Name
1.0	2008-02-19	first version	WBU

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